Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	10/037,909	KIM, YOUNG-WAN	
	Examiner	Art Unit	
	John P Trimmings	2133	

All Participants:

(1) *John P Trimmings*.

(2) *Frank Chau*.

Status of Application: _____

(3) _____.

(4) _____.

Date of Interview: *8 March 2005*

Time: *11:45 AM*

Type of Interview:
- ☒ Telephonic
- ☐ Video Conference
- ☐ Personal (Copy given to: ☐ Applicant ☐ Applicant's representative)

Exhibit Shown or Demonstrated: ☐ Yes ☐ No
If Yes, provide a brief description:

Part I.

Rejection(s) discussed:
Al.l

Claims discussed:
1 and 9.

Prior art documents discussed:

Part II.

SUBSTANCE OF INTERVIEW DESCRIBING THE GENERAL NATURE OF WHAT WAS DISCUSSED:
See Continuation Sheet

Part III.

☒ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview directly resulted in the allowance of the application. The examiner will provide a written summary of the substance of the interview in the Notice of Allowability.

☐ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview did not result in resolution of all issues. A brief summary by the examiner appears in Part II above.

(Examiner/SPE Signature)

(Applicant/Applicant's Representative Signature – if appropriate)

Continuation of Substance of Interview including description of the general nature of what was discussed: The examiner and applicant agree that Claims 1 and 9 are to be amended as follows:

1. (Amended) An error detecting circuit comprising:

an error data storing unit for dividing a circuit implemented in a chip into predetermined areas, and outputting a plurality of error signals in response to a plurality of state error signals,

a serial chain signal,

a lock-enable signal, and

a chip error signal,

each of the plurality of state error signals being enabled when an error occurs in a corresponding predetermined area,

the serial chain signal for reading the plurality of state error signals stored in the chip if the chip goes out of order when the error occurs in the circuit, and

the lock-enable signal for determining whether or not to preserve the plurality of state error signals; and

an error data collecting unit for outputting the chip error signal in response to the plurality of error signals output from the error data storing unit,

wherein the error data storing unit stores and outputs at least one of the plurality of state error signals and,

in response to the serial chain signal, enables confirmation of at least one of the plurality of state error signals stored in the error data storing unit by observing the chip error signal.

9. (Amended) A device for detecting an error in a circuit implemented in a chip, the device comprising:

an error data storing unit for dividing the circuit into a plurality of predetermined areas and outputting a plurality of error signals in response to a plurality of state error signals,

a serial chain signal,

a lock-enable signal, and

a chip error signal,

each of the plurality of state error signals being enabled when an error occurs in a corresponding one of the plurality of predetermined areas,

the serial chain signal for reading the plurality of state error signals stored in the chip if the chip goes out of order, and

the lock-enable signal for determining whether or not to preserve the plurality of state error signals; and

an error data collecting unit for outputting the chip error signal in response to the plurality of error signals, wherein the error data storing unit stores and outputs at least one of the plurality of state error signals through the chip error signal to specifically indicate which of the predetermined areas contain the error..